# TRANSMITTAL LETTER
## (General - Patent Pending)

Docket No. EN998073

In Re Application of: **Greenfield et al.**

| Serial No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 09/186,584 | November 5, 1998 | Richard J. Lee | 2613 |

Title: **ON-CHIP DYNAMIC BUFFER LEVEL INDICATORS FOR DIGITAL VIDEO ENCODER**

TO THE COMMISSIONER FOR PATENTS:



Transmitted herewith is:

**Appellants' Reply Brief**

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0457 (IBM)** as described below.
  - ☐ Charge the amount of
  - ☐ Credit any overpayment.
  - ☒ Charge any additional fee required.

Kevin P. Radigan
*Signature*

Dated: **June 17, 2003**

**Kevin P. Radigan, Esq.**
**Reg. No. 31,789**
**Heslin Rothenberg Farley & Mesiti P.C.**
**5 Columbia Circle**
**Albany, NY 12203**
**Telephone: (518) 452-5600**
**Facsimile: (518) 452-5579**

I certify that this document and fee is being deposited on **June 17, 2003** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kevin P. Radigan
*Signature of Person Mailing Correspondence*

**Kevin P. Radigan**
*Typed or Printed Name of Person Mailing Correspondence*

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Greenfield et al. : Group Art Unit: 2613

Serial No.: 09/186,584 : Examiner: Richard J. Leé

Filed: November 5, 1998 : Appeal No.:



For: ON-CHIP DYNAMIC BUFFER LEVEL INDICATORS FOR DIGITAL VIDEO ENCODER

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, on June 17, 2003.

Kevin P. Radigan

Kevin P. Radigan, Esq.
Attorney for Appellants
Reg. No. 31,789

Date of Signature: June 17, 2003

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**Appellants' Reply Brief**

Dear Sir:

This Reply Brief is being timely filed in triplicate pursuant to 37 C.F.R. §1.193(b) in rebuttal to certain characterizations and conclusions set forth in the Examiner's Answer mailed April 17, 2003, for the above-designated appeal.

## Remarks

Appellants respectively traverse the conclusion contained at page 8, paragraph 11 of the Examiner's Answer that the fullness of the external buffer BF in Greenfield et al. would inherently have to be continuously monitored. Obviously, the fullness of the buffer in Greenfield et al. is monitored, but not continuously monitored, or more specifically to the claimed invention, not continuously obtained. Appellants wish to emphasize that the present invention arose from Appellants' identifying of a deficiency of the Greenfield et al. teachings in this respect. The Declaration of Agnes Y. Ngai supports this conclusion.

Appellants' specification notes that a disadvantage of the Greenfield et al. approach is that it is implemented in microcode, and therefore, buffer fullness is not continuously obtained (see specification, p. 14, line 31 - p. 15, line 2). Without a continuous view of the fullness of the buffer, the host processor must wait until the microcode goes in, polls the on-chip register and calculates the fullness of the FIFO. This created a latency issue with the Greenfield et al. approach that resulted in an inherent inaccuracy in the FIFO fullness reading (see specification, p. 15, lines 2-7). The present invention arose from appellants' identifying of this deficiency of the Greenfield et al. teachings.

Further, appellants respectively submit that Greenfield et al. is incapable of continuously obtaining the real time fullness of the external buffer. The Greenfield et al. microcode approach to buffer fullness calculation includes a sequence of instructions. Since Greenfield et al. must execute a sequence of instructions, the buffer fullness that is known at the end of processing this sequence of instructions is not known during the processing of the sequence. In other words, while the processor is doing the updating of the buffer level indicator, a true (i.e., instantaneous) buffer level signal is not returned on a continuous basis. As one example, in the Greenfield et al. system, a buffer level indicator would be returned approximately once per macroblock or per picture frame. In

contrast, appellants' hardware logic continuously obtains the fullness of the external buffer.

As a further characterization, claims 32 & 34 (for example) recite that the continuous obtaining includes obtaining the fullness of the external buffer (BF) every cycle of the encoder. Clearly, this continuous obtaining of the external fullness every encoder cycle is quite different from the buffer indicator obtained by Greenfield et al. Since the Greenfield et al. buffer fullness calculation includes a sequence of instructions, and only one instruction may be, for instance, executed per encoder cycle, the microcode cannot obtain the buffer fullness every encoder cycle (see Ngai Declaration, p. 3, line 6). Thus, in Greenfield et al., the actual fullness of the buffer is not continuously obtained every cycle, as recited in these claims.

For the above-stated reasons, as well as for those set forth in the Appeal Brief, appellants respectively request reversal of all rejections.

Respectfully submitted,

Kevin P. Radigan

Kevin P. Radigan
Reg. No. 31, 789
Attorney for Appellants

Dated: June 17, 2003

HESLIN ROTHENBERG FARLEY & MESITI, P.C.
5 Columbia Circle
Albany, New York 12203
Telephone: (518) 452-5600
Facsimile: (518) 452-5579